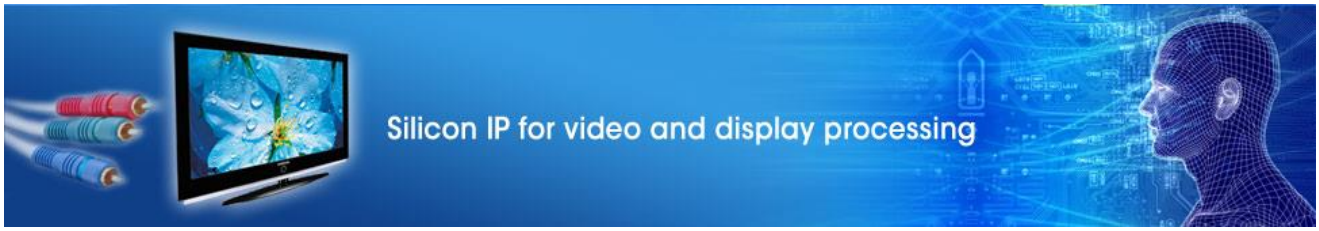


VPC-6 Silicon IP Core

Linear Frame Rate Converter

Overview

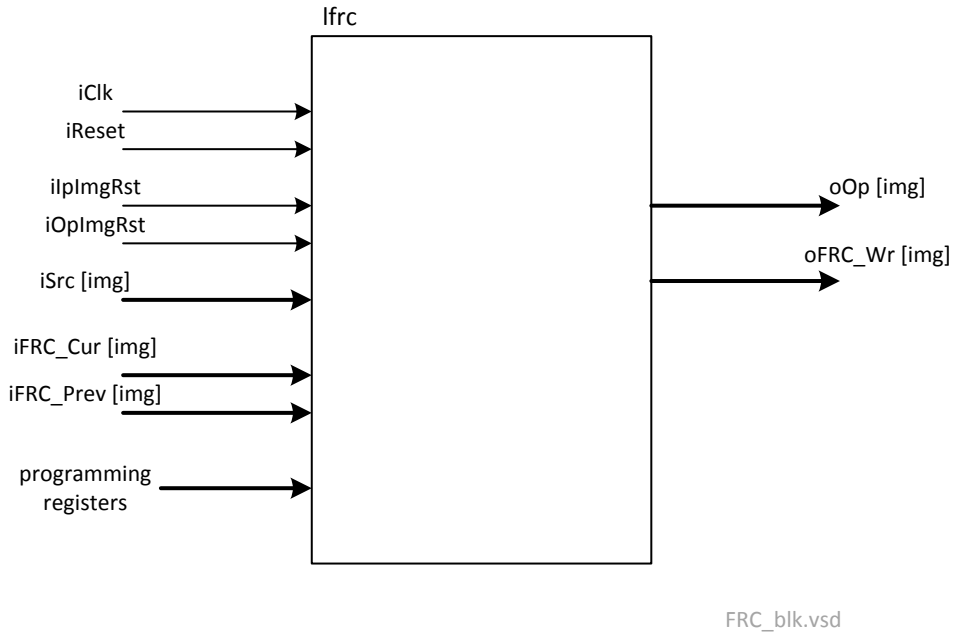
The VPC-6 is a linear frame rate converter used to convert between frame rates while maintaining the appearance of smooth motion. Frame rate conversion by simply dropping or repeating frames has low complexity, but can result in severe motion judder. Motion compensated techniques can preserve fluidity, but are complex and expensive to implement. Using weighted contributions from adjacent video frames, the VPC-6 avoids motion judder associated with drop/repeat without the cost or complexity of motion compensation. When used in conjunction with the CXC-1 Configurable Cross Converter, the latter provides a complete system level wrapper including DRAM interface and seamless integration with other Crucial IP cores.

The VPC-6 is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A VPC-6 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the VPC-6 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - Linear frame rate converter reduces motion judder without the complexity of motion compensation
  - Ideal for 50/60 Hz and 60/50 Hz standards conversion
  - Supports progressive formats up to 1080p
  - Supports interlaced input formats when used with VPC-1 Deinterlacer IP core
  - Supports interlaced output formats when used with VSC-1 Scaler IP core
  - Phase of current frame calculated automatically based input/output skew
  - Programmable LUT provides range of intermediate settings between simple drop/repeat and fully linear FRC
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
- **DRAM Interface**
  - CXC-1 wrapper provides all circuitry required to interface seamlessly with Xilinx and Altera memory controllers
- **Compatibility**
  - CXC-1 wrapper provides seamless integration with other Crucial IP cores
  - Support for both Xilinx and Altera devices



VPC-6 Block Diagram

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support