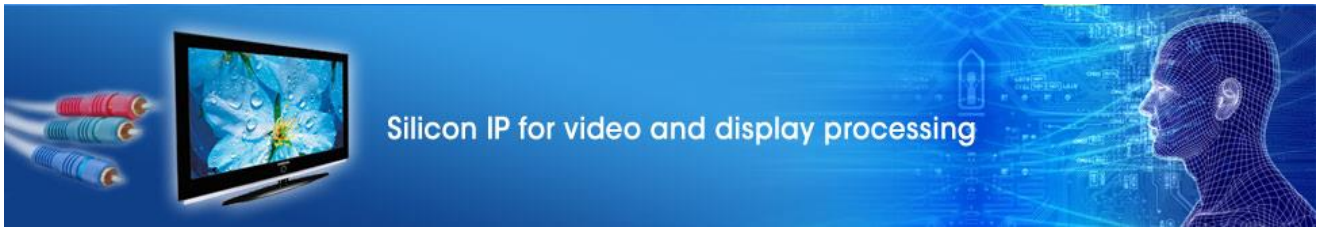


VSC-2 Silicon IP Core

Video Scaler with Electronic Keystone Correction

Overview

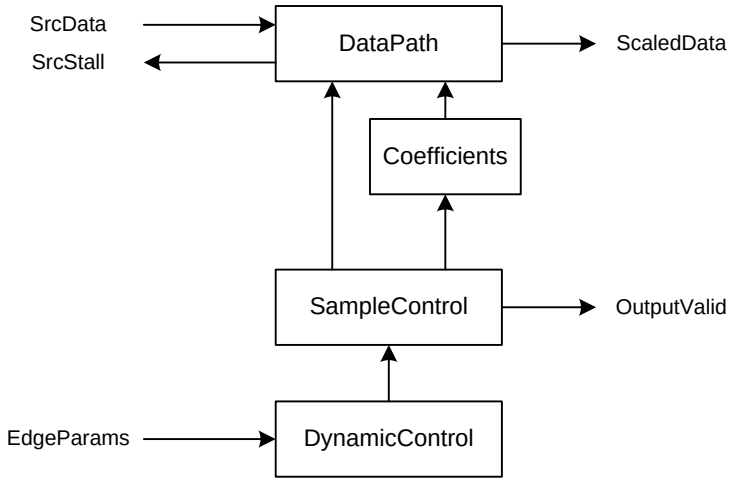
The VSC-2 is a high quality polyphase scaler including electronic keystone correction which has been optimized for video and graphics applications. The scaler may be used in conjunction with the VPC-1 Video Processor and Deinterlacer IP core or with any other customer or third party IP. Support for both shrink and zoom modes allows full screen display of any video or graphics source as well as arbitrary resizing for PIP applications. Dynamically loadable coefficients provide maximum flexibility to further optimize for different sources types and to enable effects such as image sharpening. In addition, the core includes a number of Verilog parameters that allow it to be tailored at build time to satisfy specific requirements. Flexibility, robust design and rigorous testing combine to make the VSC-2 ideal for both consumer electronic and projection applications.

The VSC-2 includes complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

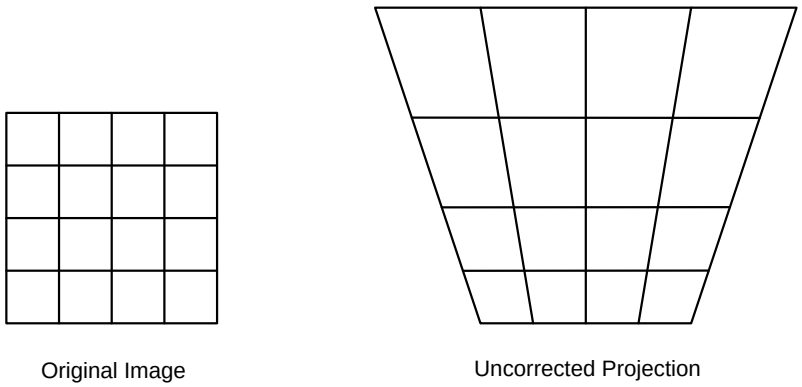
The VSC-2 is available on Crucial IP's FPGA development platform for demonstration and evaluation purposes. The platform includes a microcontroller to facilitate control of the IP core from a host PC. Perl scripts are provided for ease of setup and serve as clear templates for the programming model. An interactive monitor program is also included.

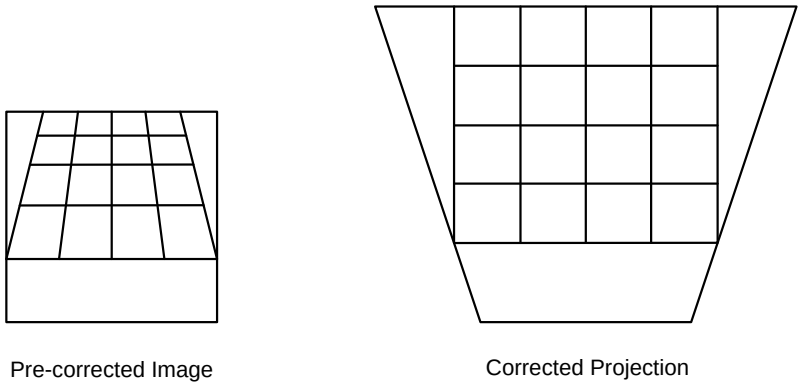
Features

- **General**
  - High quality polyphase scaler optimized for video and graphics applications
  - Separate horizontal and vertical scalers
  - Supports both shrink and zoom modes
  - 8/10-bit 4:2:2 or 4:4:4 processing
  - Memory and gate efficient implementation
  - Fully synchronous design
- **Scaling**
  - High quality polyphase scaling
  - Arbitrary horizontal and vertical scale factors
- **Keystone Correction**
  - Electronic vertical keystone correction
  - Correct filtering and sub-pixel accuracy avoids jaggies during keystone correction
  - Geometrically accurate correction in both horizontal and vertical dimensions
  - Scale factors calculated automatically in realtime
  - Supports crossing of shrink/zoom boundary in keystone mode
- **Programmability**
  - Dynamically loadable coefficients for flexible image quality (coefficients may also be fixed if desired)
  - Optional image sharpening
  - Scale factors and keystone correction dynamically alterable without display artifacts



VSC-2 Block Diagram (Horizontal or Vertical)





Vertical Keystone Correction

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support

FPGA Development Platform

The development platform consists of the following components:

- Altera EP3C120F780 development board
- Bitec HSMC quad video daughter card
- Bitec HSMC DVI daughter card

The development platform provides the following functionality for demonstration and evaluation purposes:

- Composite, S-video and DVI inputs
- DVI output with display resolution configurable up to 1080p
- Interlaced sources converted to progressive format using VPC-1 deinterlacer core
- Video/graphics sources appear as scalable window in DVI display
- Optional electronic keystone correction of output image
- I2C interface to FPGA via external USB adaptor
- Monitor program and Perl scripts for ease of setup