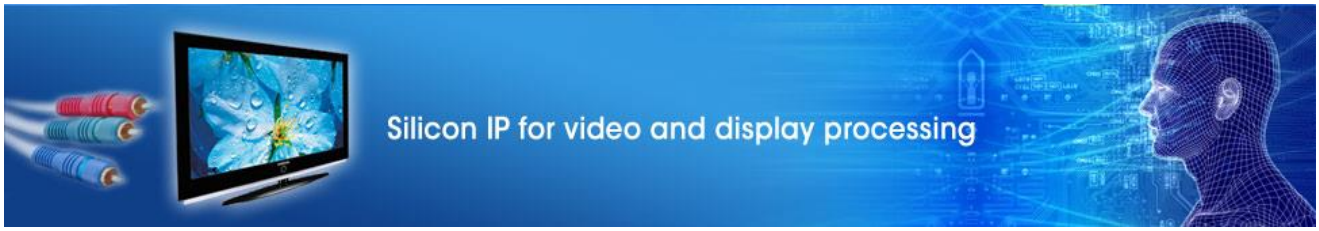


VSC-1 Silicon IP Core

Video Scaler with Shrink and Zoom Support

Overview

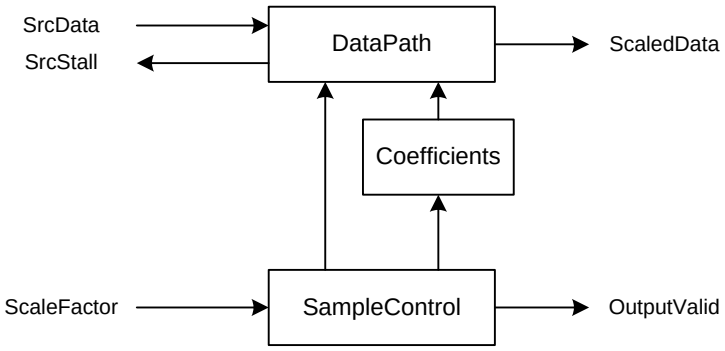
The VSC-1 is a high quality polyphase scaler which has been optimized for video and graphics applications. The scaler may be used in conjunction with the VPC-1 Video Processor and Deinterlacer IP core or with any other customer or third party IP. Support for both shrink and zoom modes allows full screen display of any video or graphics source as well as arbitrary resizing for PIP applications. Dynamically loadable coefficients provide maximum flexibility to further optimize for different sources types and to enable effects such as image sharpening. In addition, the core includes a number of Verilog parameters that allow it to be tailored at build time to satisfy specific requirements. Flexibility, robust design and rigorous testing combine to make the VSC-1 ideal for both consumer electronic and broadcast applications.

The VSC-1 is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A VSC-1 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the VSC-1 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - High quality polyphase scaler optimized for video and graphics applications
  - Separate horizontal and vertical scalers
  - Supports both shrink and zoom modes
  - Dynamic resizing and aspect ratio conversion (ARC) without artifacts
  - Selective crop and zoom (Ultra Zoom)
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
- **Scaling**
  - High quality polyphase scaling
  - Arbitrary horizontal and vertical scale factors
  - Correct filtering minimizes artifacts at all scale factors
- **Programmability**
  - Dynamically loadable coefficients for flexible image quality
  - Optional image sharpening
  - Scale factors dynamically alterable without display artifacts
- **Build Time Options**
  - 4:2:2 or 4:4:4 data path
  - 8, 10 or 12-bit data path precision
  - Number of taps, number of phases, coefficient precision
- **Compatibility**
  - Use standalone or in conjunction with VPC-1 Video Processor and Deinterlacer for complete up/down/cross conversion



VSC-1 Block Diagram (Horizontal or Vertical)

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support