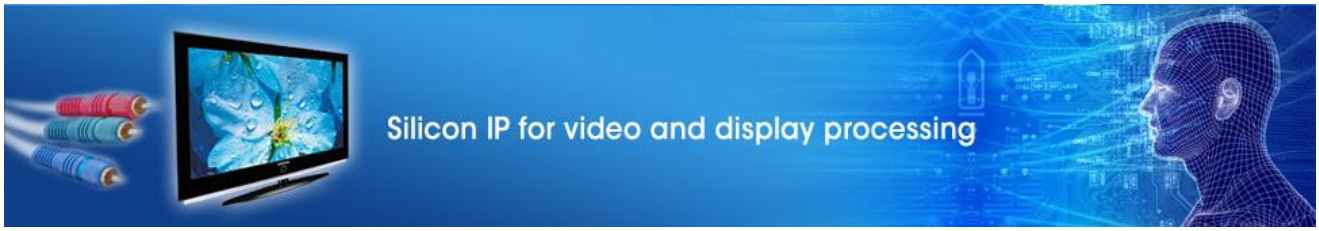


VPC-3 Silicon IP Core

Mosquito/Block Noise Reducer

Overview

The VPC-3 provides noise reduction functionality which targets both mosquito noise and block noise associated with digital compression. Mosquito noise reduction reduces noise which often occurs near edges, due to quantization of DCT coefficients. Block artifact reduction detects and adaptively softens block boundaries frequently visible in regions of low variability. In either case, an advanced algorithm ensures that noise reduction is achieved with minimal undesired loss of detail. Automatic detection of block boundaries means that no prior knowledge of video format or block alignment is required. When combined with the Gaussian noise reduction feature of the VPC-1 Deinterlacer IP core, a complete noise reduction suite is provided to address most types of noise.

The VPC-3 is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

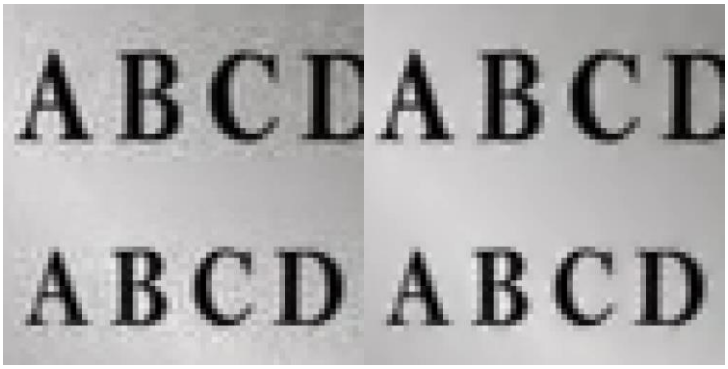
A VPC-3 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the VPC-3 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - The following input formats are supported: 480i, 576i, 480p, 576p, 720p, 1080i, 1080p and other custom formats
  - Compatible with both progressive and interlaced sources
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
  - Low latency (~5 lines)
  - Fully synchronous design

- **Noise Reduction**
  - Reduces mosquito noise associated with digital compression
  - Detects and adaptively softens block boundaries frequently visible in regions of low variability
  - Separately controllable levels for both Mosquito Noise Reduction and Block Artifact Reduction
  - Minimizes undesired loss of detail
  - When combined with the Gaussian noise reduction feature of the VPC-1 Deinterlacer, a complete noise reduction suite is provided

- **Compatibility**
  - Use standalone or in conjunction with VPC-1 Deinterlacer or other third party IP
  - Support for both Xilinx and Altera devices



Mosquito Noise Reduction (Actual Capture)

Block Artifact Reduction (Actual Capture)

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support