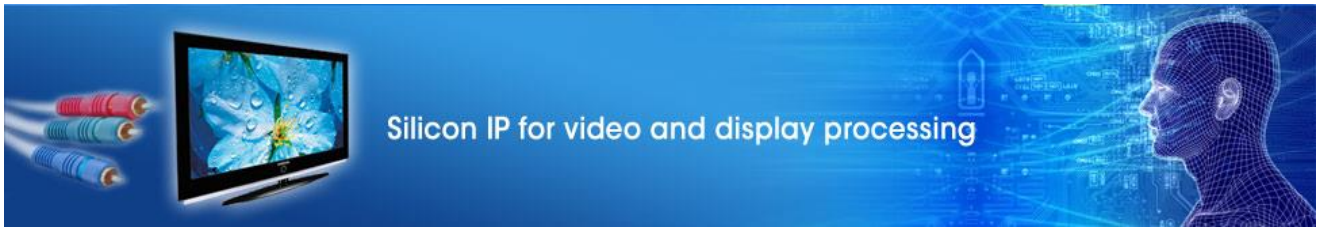


VPC-1 Silicon IP Core

Video Processor and Deinterlacer with Line-Doubled Output

Overview

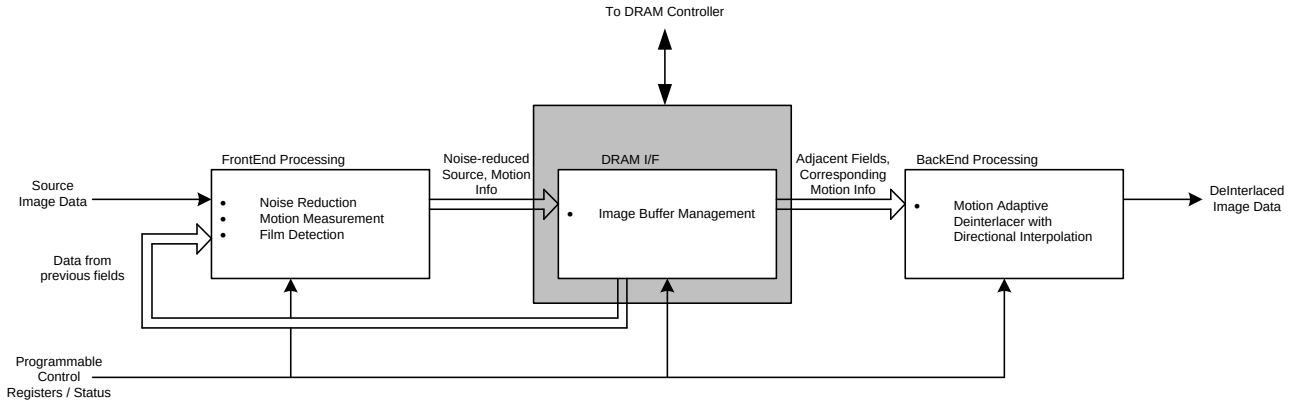
The VPC-1 is a high quality motion adaptive deinterlacer and video processor with line-doubled output. Additional functions include motion adaptive noise reduction, low angle directional interpolation and film cadence detection (supports multiple cadences including 3:2, 2:2 and others). When combined with Crucial IP's VSC-1 scaler core, the VPC-1 can be used to provide complete up/down/cross conversion. Years of experience in developing video processing algorithms have contributed to the outstanding performance of the VPC-1 amongst motion adaptive class solutions. The full feature set, robust performance and extremely efficient implementation make the VPC-1 ideal for both consumer electronic and broadcast applications.

The VPC-1 is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A VPC-1 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the VPC-1 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - The following input formats are supported: 480i, 576i, 480p, 576p, 720p, 1080i, 1080p and other custom formats
  - Line-doubled output (interlaced sources)
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
  - Low latency algorithm avoids lip sync problems (latency can be set to 0, 1 or 2 fields plus approximately 20 lines)
- **Deinterlacing**
  - High quality motion adaptive deinterlacer
  - Excellent stability in presence of noise and at onset of motion
- **Low angle directional interpolation**
  - Eliminates jaggies on moving diagonal edges, even those at angles close to the horizontal
- **Film detection**
  - Robust detection and processing of multiple cadences including 3:2, 2:2, 2:2:2:4, 2:3:3:2, 3:2:3:2:2, 5:5, 6:4 and 8:7
  - Bad edit detection with no incorrectly displayed frames under normal conditions
- **Noise reduction**
  - Motion adaptive temporal noise reduction reduces Gaussian noise without loss of spatial resolution
  - Works with progressive sources
- **Compatibility**
  - Support for both Xilinx and Altera devices



VPC-1 Block Diagram

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support