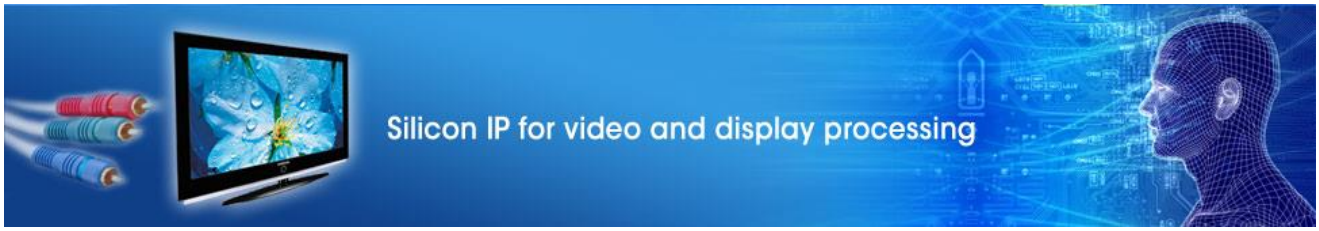


CXC-1 Silicon IP Core

Configurable Cross Converter

Overview

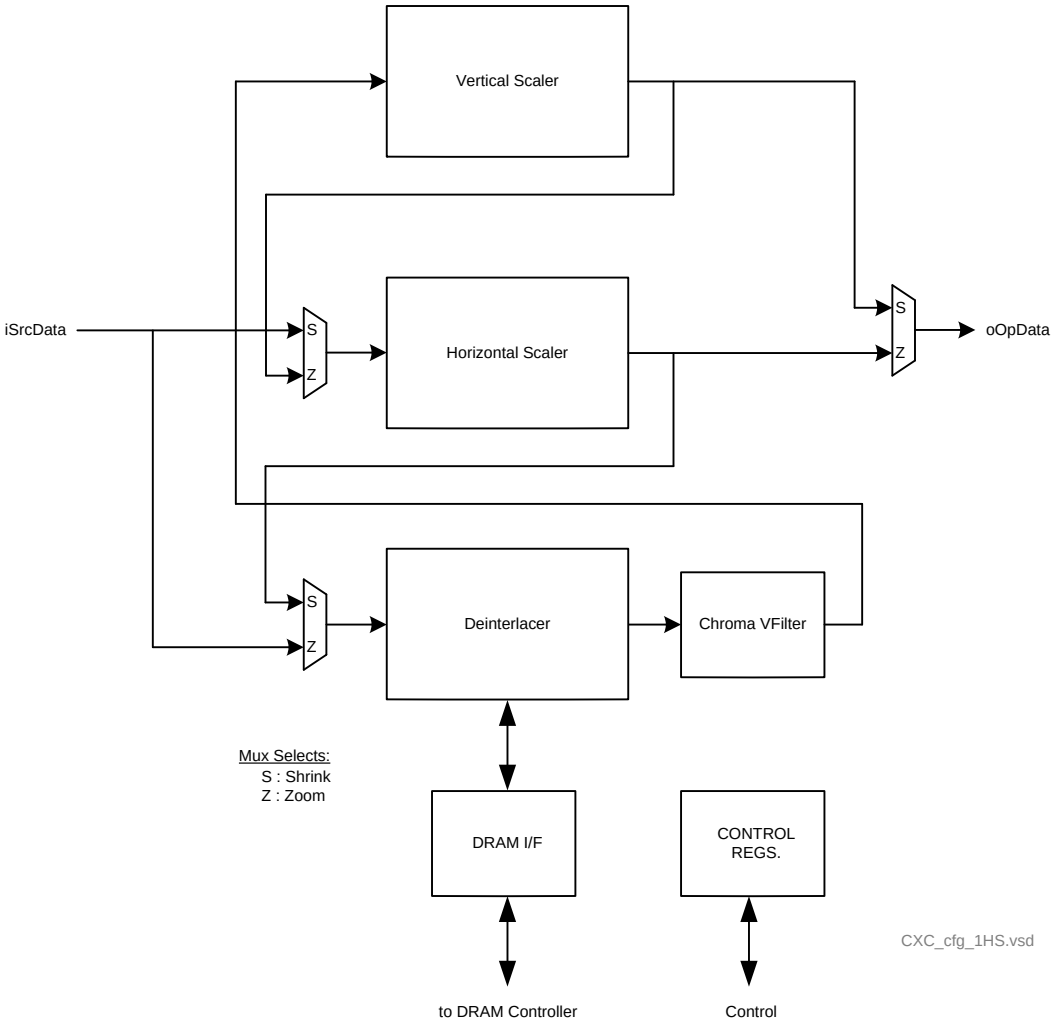
The CXC-1 is a parameterized integration of the VPC-1 Deinterlacer and VSC-1 Scaler IP cores along with all circuitry necessary to interface to a DRAM controller. The CXC-1 greatly simplifies using the VPC-1 and VSC-1 in a wide range of applications. All build-time parameters supported by the VPC-1 and VSC-1 are available at the top level of the CXC-1. Additional build-time parameters are provided to include or exclude certain processing blocks. This allows, for example, the CXC-1 to be configured as a full up/down/cross converter or as a deinterlacer only or a scaler only. When used to perform up/down/cross conversion, the location of certain blocks are dynamically switchable to minimize DRAM bandwidth. An additional parameter instantiates circuitry as required for dynamic resizing without artifacts. While many of the above features were previously illustrated through the use of reference designs, the CXC-1 provides a highly flexible system in one easy to use and fully supported IP core.

The CXC-1 is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A CXC-1 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. The design includes a built-in user interface with embedded OSD to simplify access to key features of the IP. In addition to simplifying the evaluation of the CXC-1 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - Parameterized integration of VPC-1 deinterlacer and VSC-1 scaler IP cores with flexibility to address wide range of applications
  - Complete up/down/cross conversion (the following input and output formats are supported: 480i, 576i, 480p, 576p, 720p, 1080i, 1080p and other custom formats)
  - Dynamic resizing and real time aspect ratio conversion (ARC) without artifacts
  - Selective crop and zoom (Ultra Zoom)
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
- **Deinterlacing**
  - High quality motion adaptive deinterlacing and related functions based on VPC-1 Deinterlacer IP core
- **Scaling**
  - High quality polyphase scaling based on VSC-1 Scaler IP core
- **DRAM Interface**
  - Includes all circuitry required to interface seamlessly with Xilinx and Altera memory controllers
- **Compatibility**
  - Support for both Xilinx and Altera devices



CXC-1 Block Diagram

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support