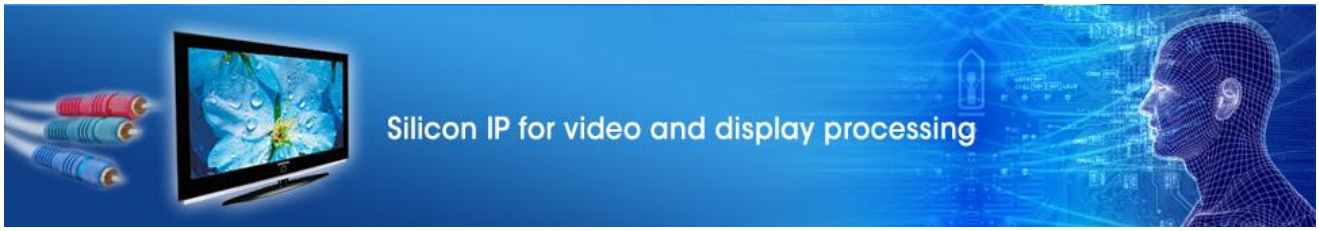


CMV-1 Silicon IP Core

Configurable Multi-Viewer

Overview

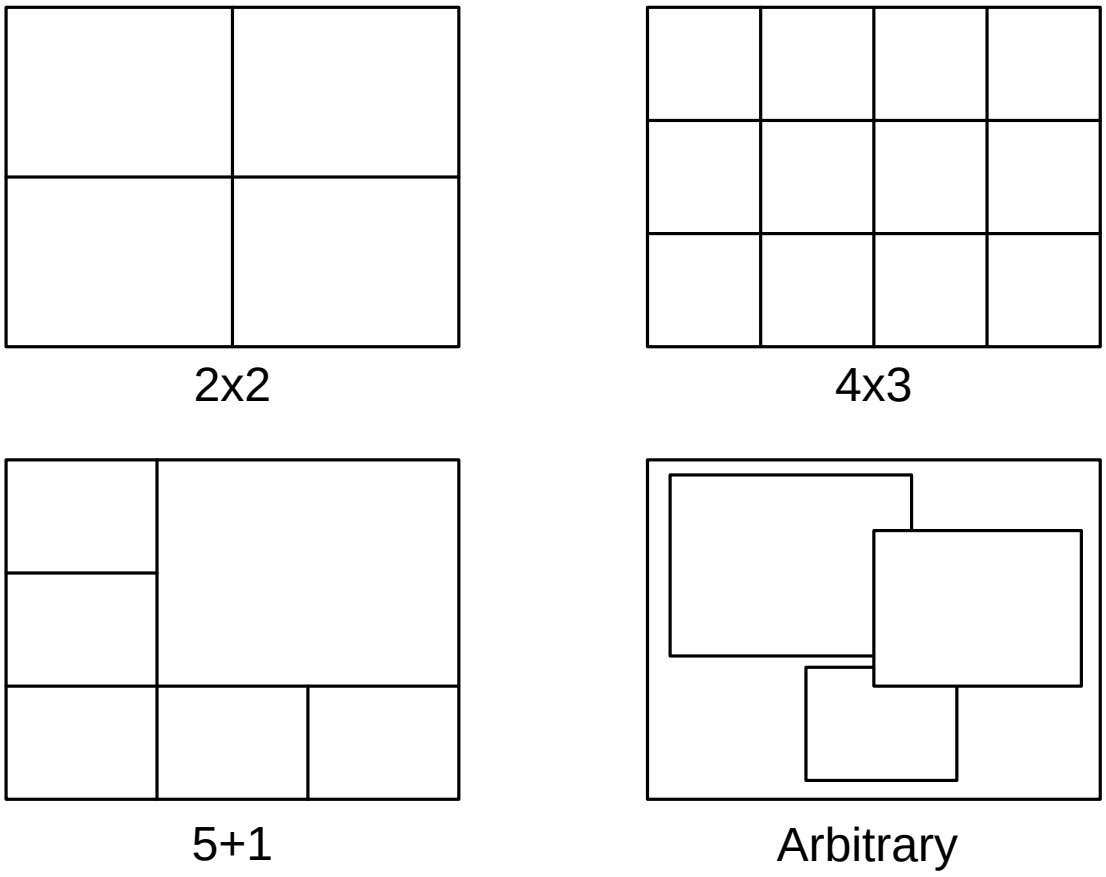
The CMV-1 is a parameterized integration of the VSC-1 Scaler, VPC-1 Deinterlacer and other IP as required for multi-viewer applications. The CMV-1 greatly simplifies the development of multi-viewer applications while allowing flexible system design through the use of Verilog build-time parameters. For instance, the system may be configured to allow for up to 32 video sources and one or more display outputs. For cost sensitive applications, spatial deinterlacing of interlaced inputs is provided by the VSC-1 Scaler. For higher quality applications, one or more instances of the VPC-1 Deinterlacer may optionally be used. In addition to deinterlacing, scaling and arbitrary placement of multiple video sources, a bit-mapped OSD is provided to overlay graphics and text for a professional looking display. Various layering effects including blending and transparency are also supported. Low level software support and example application code minimize customer development effort and reduce time to market for multi-viewer applications.

The CMV-1 is available with complete Verilog source code, Verilog test bench and bit-accurate C models as part of the license. Integration and programming guidelines are also included backed up by expert technical support.

A CMV-1 reference design is available for standard development kits from Xilinx and Altera for demonstration and evaluation purposes. In addition to simplifying the evaluation of the CMV-1 IP core, the design also serves as a template for customer application development.

Features

- **General**
  - Parameterized integration of VSC-1 Scaler and VPC-1 Deinterlacer IP cores for flexible multi-viewer applications
  - Up to 32 independent video sources and multiple video displays
  - Flexible image size and positioning for each window
  - Layering effects including blending, transparency and overlap
  - Support for 4K sources and displays (future release)
  - 8/10/12-bit 4:2:2 or 4:4:4 processing
- **Video Processing**
  - Low cost deinterlacing/scaling provided by VSC-1 Scaler IP core
  - High quality deinterlacing optionally provided by VPC-1 Deinterlacer IP core
- **OSD**
  - Flexible bit-mapped OSD
  - Software support for rendering of 2D graphics and text
- **Compatibility**
  - Support for both Xilinx and Altera devices



CMV-1 Example Layouts

Design Deliverables

The following deliverables are included with the license:

- Synthesizable Verilog RTL source code (encrypted or unencrypted as per license agreement)
- Verilog testbench
- Bit-accurate C model
- Verification test suite
- Product documentation
- Integration guidelines
- Integration support

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